ABSTRACT OF DISCLOSURE

A semiconductor memory device with an improved redundancy scheme is provided. The semiconductor memory device includes at least one memory block having a plurality of memory banks that are arranged in a column direction. Each memory bank includes a plurality of normal memory cells, which are arranged according to a row and column structure, and at least one redundancy memory cell to replace defective memory cells. At least one memory bank, adjacent to an edge of photo shot or an edge of chip, among the plurality of memory banks includes more redundancy lines than the other memory banks. In the semiconductor memory device, when memory banks have different numbers of defective memory cells to be repaired, the number of redundancy memory cells of each memory bank is differently set, thus increasing the yield.

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